

## WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
  - a wiring substrate having a first surface, a second surface opposed to the first surface, and an opening portion extending from the first surface to the second surface;
  - a terminal formed on the first surface;
  - a wiring formed on the second surface and having one end portion projected to the opening portion and electrically connected to the terminal;
- 10 a first semiconductor element having a third surface formed with a first external terminal and an internal connection terminal outside of the first external terminal, and a fourth surface opposed to the third surface, the first semiconductor element being received in the opening portion such that the internal connection terminal is placed on and electrically connected to the inner end portion of the wiring;
- 15 a second semiconductor element having a fifth surface formed with an electrode, and a sixth surface opposed to the fifth surface, the sixth surface being attached on the fourth surface;
- 20 a conductor electrically connecting the electrode of the second semiconductor element and the terminal of the wiring substrate; and
- 25 a sealing member sealing the first and second semiconductor elements and the conductor.

  

2. A semiconductor device according to claim 1, wherein the first semiconductor element is formed by a wafer-level chip size package in which the internal connection terminal and the first external terminal are relocated by redistribution wiring from an internal electrode being coated in an insulating layer.

3. A semiconductor device according to claim 1, wherein the terminal and the wiring on the wiring substrate are electrically connected to each other via a through hole.

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4. A semiconductor device according to claim 1, further comprising a second external terminal projected on the second surface of the wiring substrate and electrically connected to the wiring.

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5. A semiconductor device according to claim 1, wherein the second semiconductor element comprises a plurality of chips and are mounted on the fourth surface of the first semiconductor element.

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6. A semiconductor device according to claim 1, wherein a plurality of wirings are formed on the second surface of the wiring substrate, and inner end portions thereof are arranged in staggered form and projected into the opening portion.

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7. A semiconductor device according to claim 1, wherein the second surface of the wiring substrate and the wiring on the second surface are covered with an insulating film.

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8. A semiconductor device according to claim 6, wherein connecting portions each between the inner end portion of the wiring and the internal connection terminal are covered with an insulating member.

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9. A semiconductor device comprising:  
a wiring substrate having a first surface, a second

surface opposed to the first surface, and a substantially centrally located aperture extending from the first surface to the second surface;

5 a bonding post formed on the first surface near the aperture;

a conductive trace formed on the second surface and having one end projected to the aperture and electrically connected to the bonding post;

10 a first semiconductor chip having a third surface formed with a first terminal and a second terminal outside of the first terminal, and a fourth surface opposed to the third surface; the first semiconductor chip being received in the aperture such that the second terminal is placed on and electrically connected to the one end of the conductive 15 trace;

a second semiconductor chip having a fifth surface formed with an electrode pad, and a sixth surface opposed to the fifth surface, the sixth surface being attached to the fourth surface;

20 a bonding wire electrically connecting the electrode pad of the second semiconductor chip and the bonding post of the wiring substrate; and

a sealing member sealing the first and second semiconductor chips and the bonding wire.

25 10. A semiconductor device according to claim 9, wherein the first semiconductor chip comprises a chip size package in which the first and second terminals are relocated by redistribution wiring from an electrode pad being coated 30 in an insulating layer.

11. A semiconductor device according to claim 9, wherein the bonding post and the conductive trace on the

wiring substrate are electrically connected to each other via a through hole.

12. A semiconductor device according to claim 9,  
5 further comprising a third terminal formed on the second surface of the wiring substrate and electrically connected to the conductive trace.

13. A semiconductor device according to claim 9,  
10 wherein the second semiconductor chip comprises a plurality of chips and are mounted on the fourth surface of the first semiconductor chip.

14. A semiconductor device according to claim 9,  
15 wherein a plurality of conductive trace are formed on the second surface of the wiring substrate, and a plurality of one ends thereof are arranged in staggered form and projected into the aperture.

20 15. A semiconductor device according to claim 9,  
wherein the second surface of the wiring substrate and the conductive trace on the second surface are covered with an insulating film.

25 16. A semiconductor device according to claim 14,  
wherein connecting portions each between the one end portion of the conductive trace and the second terminal are covered with an insulating member.

30 17. A semiconductor device comprising:  
a base substrate having a first surface, a second surface opposed to the first surface, and a substantially centrally located aperture extending from the first surface

to the second surface;

a plurality of bonding posts formed on the first surface along the aperture;

5 a plurality of conductive traces formed on the second surface and electrically connected to the bonding post, each of the conductive traces having one end projected to the aperture and the other end located at the second surface;

10 a first semiconductor element having a third surface formed with first terminals located at the center of the third surface and second terminals located at the periphery of the third surface, and a fourth surface opposed to the third surface, the first semiconductor element being received in the aperture and being supported by the one ends of the conductive traces;

15 a second semiconductor element having a fifth surface formed with electrode pads, and a sixth surface opposed to the fifth surface, the sixth surface being attached to the fourth surface;

20 a plurality of bonding wires electrically connecting the electrode pads and the bonding posts; and

a sealing member sealing the first and second semiconductor elements and the bonding wire.

25 18. A semiconductor device according to claim 17, wherein the first terminals are arranged in a matrix form.

30 19. A semiconductor device according to claim 18, wherein the first semiconductor element includes a plurality of electrode pads formed on the third surface and along an edge of the first semiconductor element, and redistribution wirings coupling the first terminals and the electrode pads.

